A Delay Generation Technique for Narrow Time Interval Measurement

By: Rashid Rashidzadeh
University of Windsor

Why Narrow Time Interval Measurement ?

1. Laser-based distance measurement
2. Rise/Fall time
3. Clock skew degradation measurement in digital circuits
4. Jitter or phase noise measurement (variation of rising and falling edges of digital signals)

Possible Measurement Methods

Off-Chip Measurement

- Test channel loading effect
- Significant loss and distortion
- Large number of parameters or nodes to be monitored

On-Chip Measurement

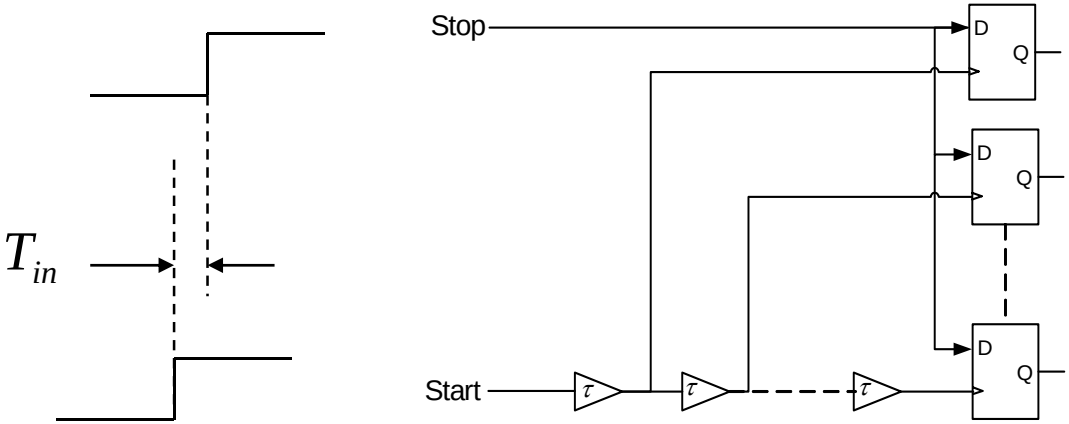
- The timing quantities to be measured are on the same magnitude as the resolution of the measurement device

Proposed Measurement Methods in the Literature

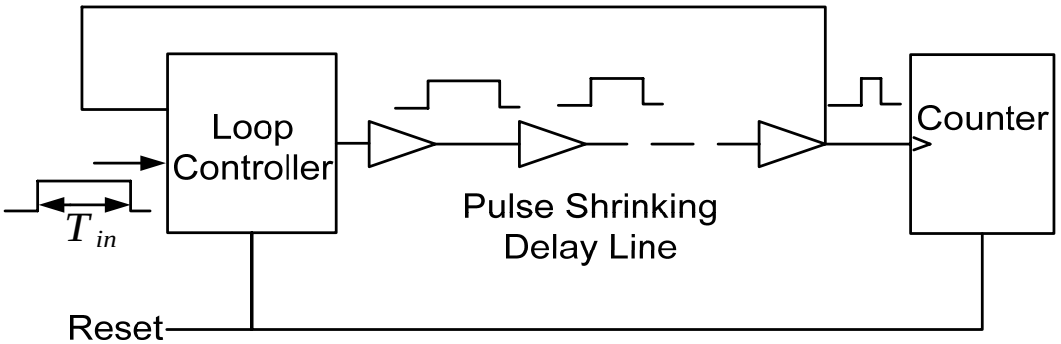
Increasing the effective measurement resolution through:
Subsampling or pulse stretching methods

(a) A delay line without a reference oscillator
(b) An interpolator with a reference oscillator
(c) Two delay lines used as a Vernier delay line or ring oscillators
(d) Time Amplifier

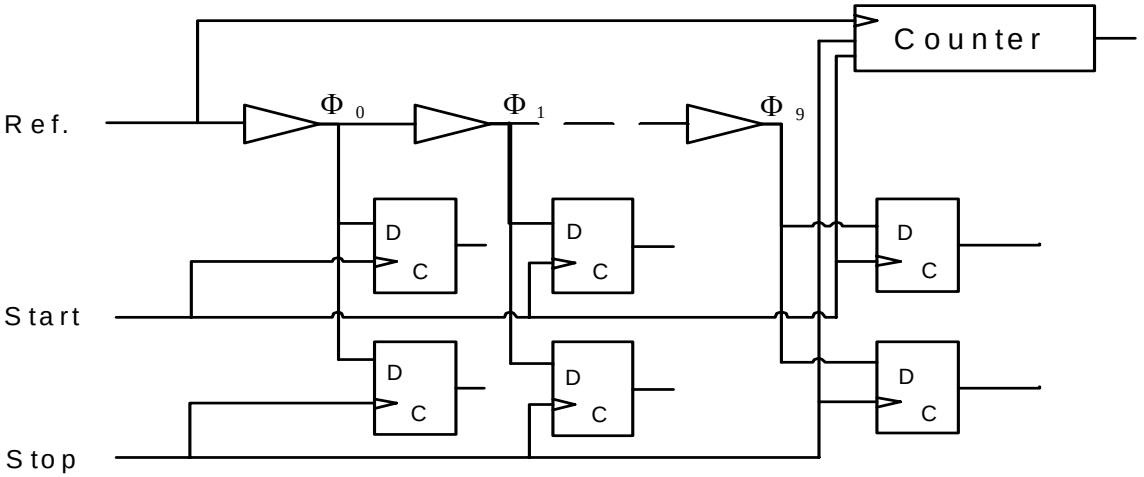
Time to Digital Conversion Using a Delay Line

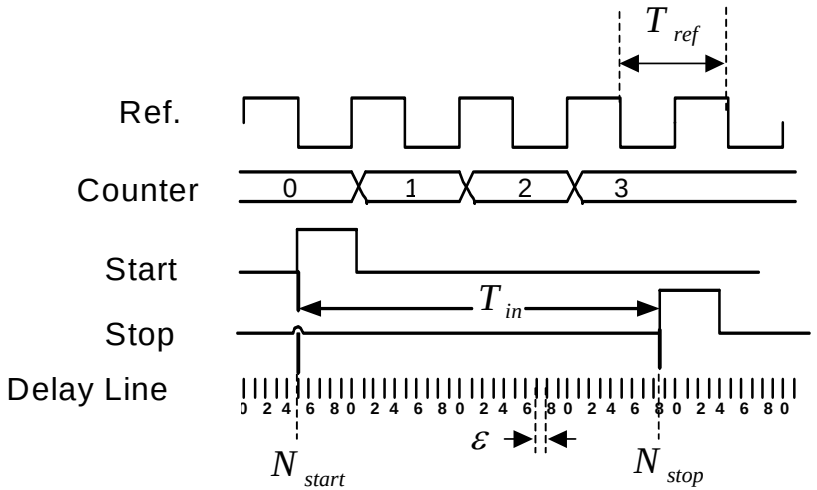


Basic Time to Digital Converter (TDC)



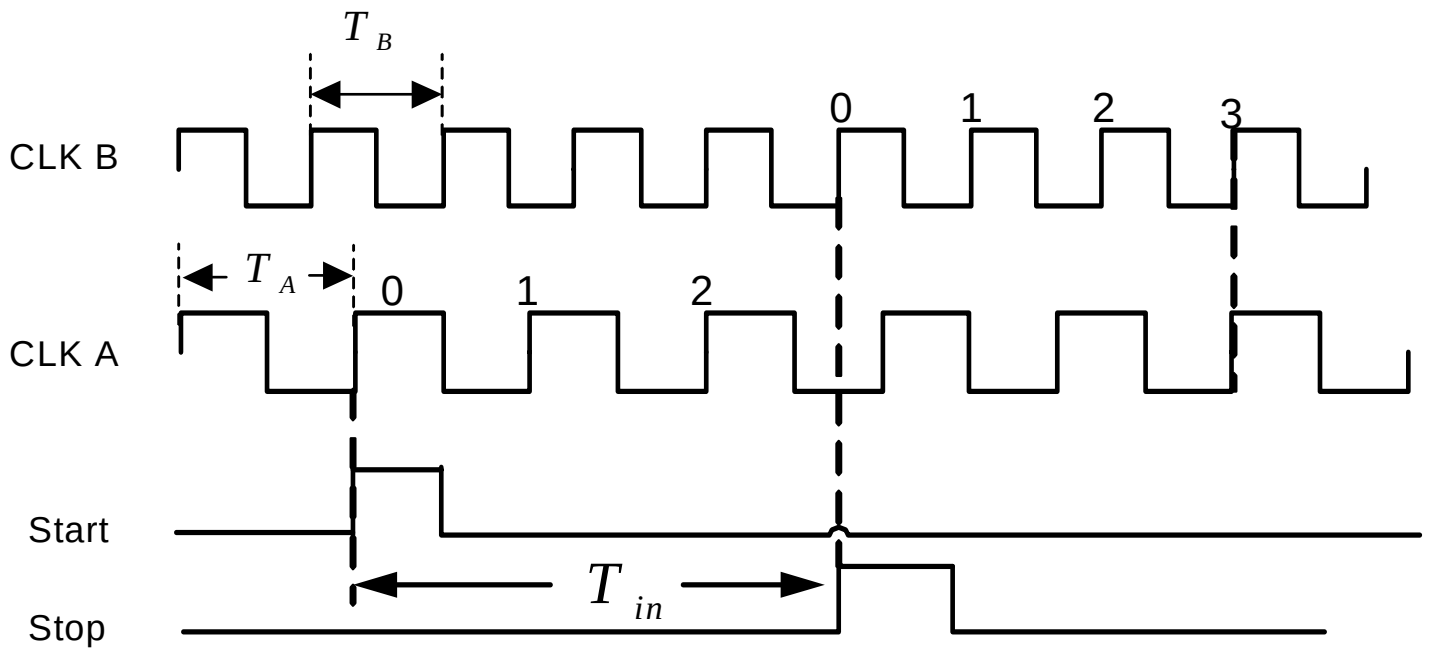
TDC Using a Reference Oscillator





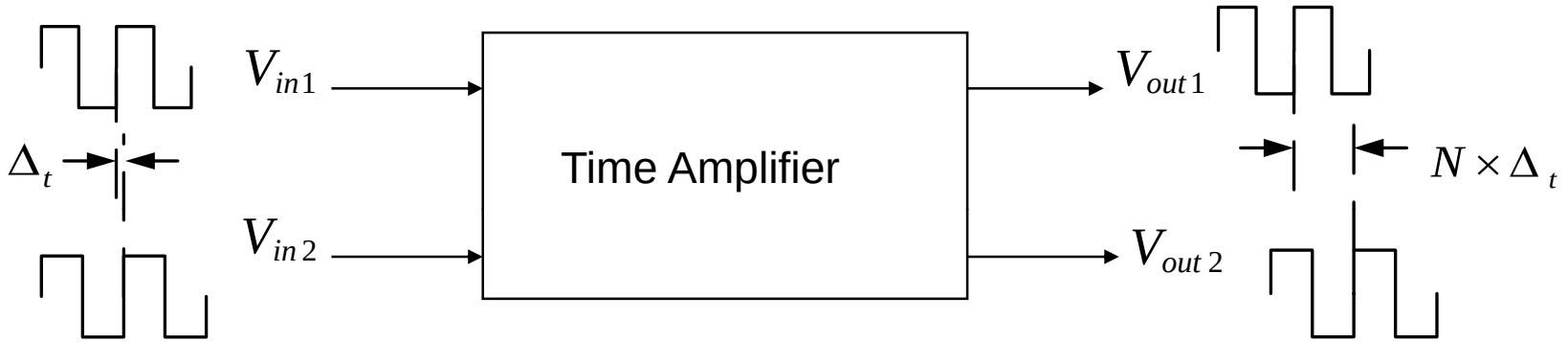
$$T_{in} = N_{ref} \times T_{ref} + (N_{Start} - N_{Stop})\varepsilon$$

Timing Diagram of TDC with Two Reference Oscillators

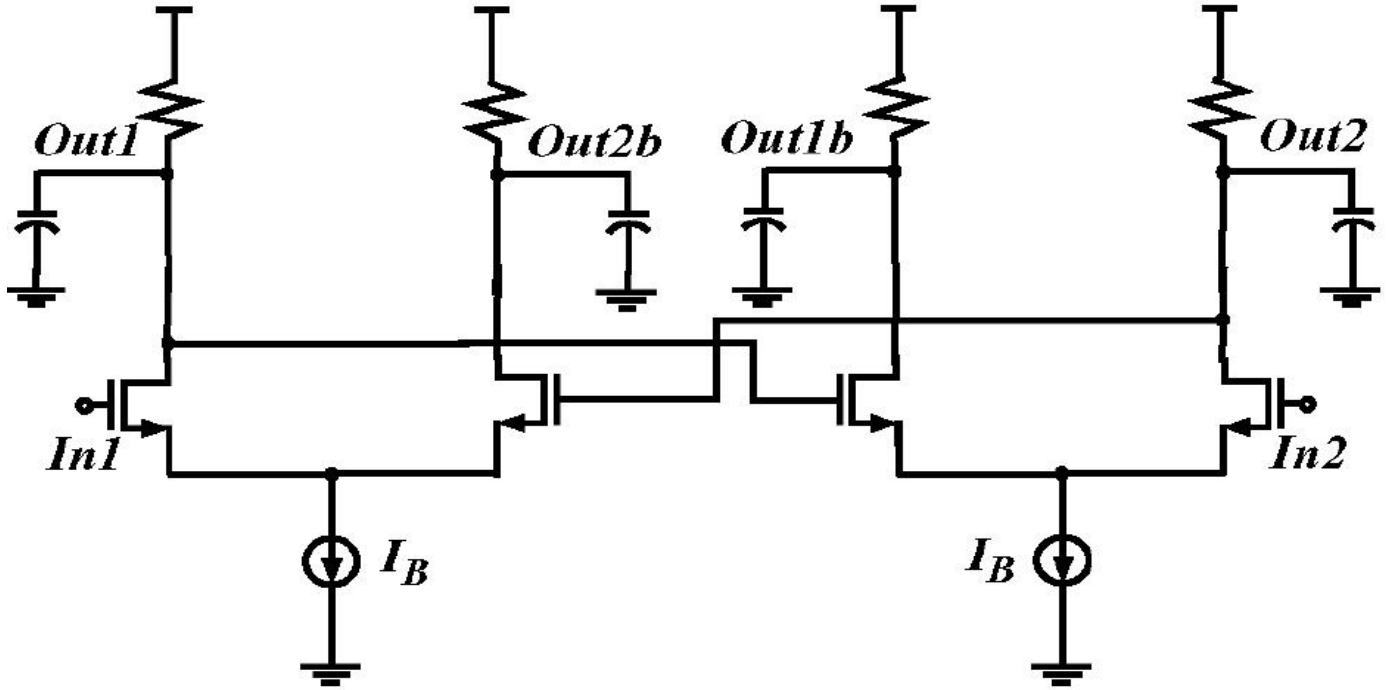


$$T_{in} = N_1 \times T_A + N_2 \times (T_A - T_B)$$

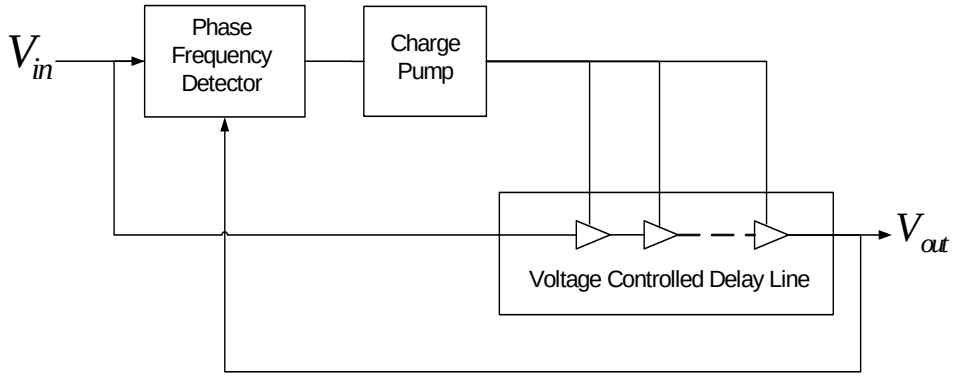
An Alternative Method of Short Time Interval Measurement

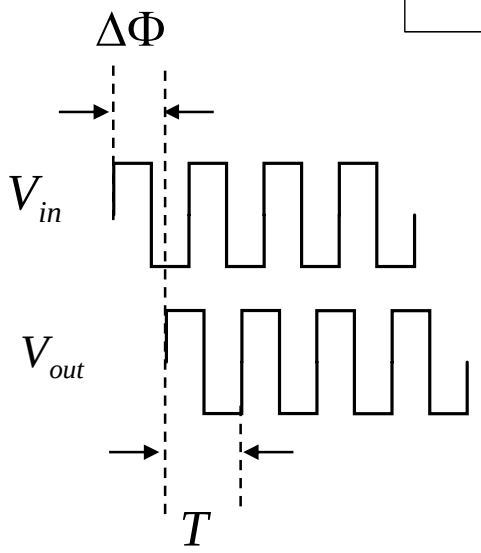


CMOS Implementation of Time Amplifier

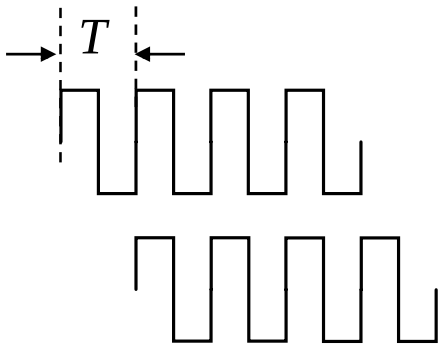


Charge Pump Delay Locked Loop (DLL)



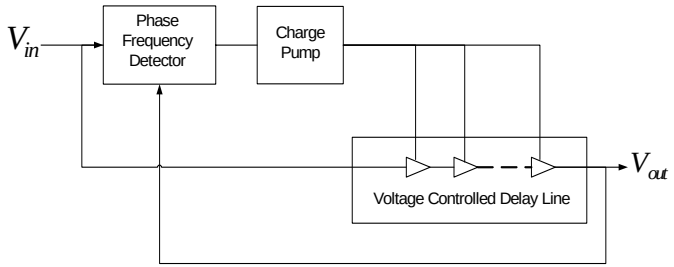


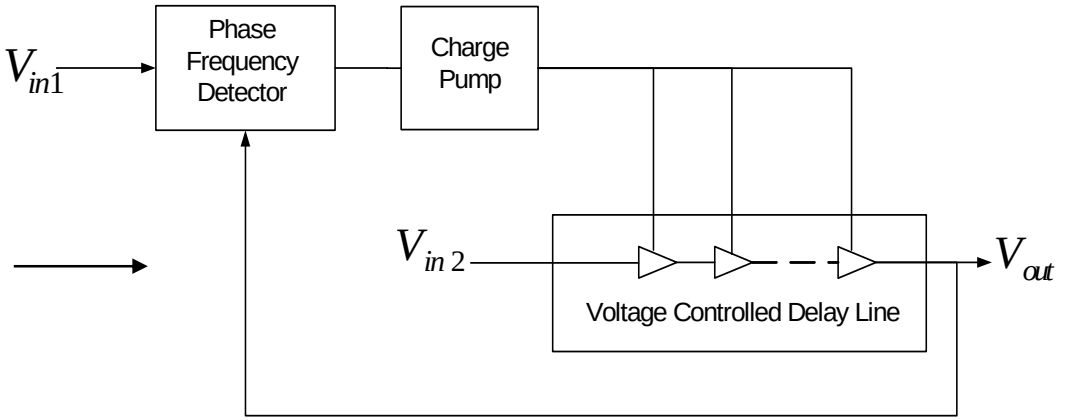
Before the Phase Lock is acquired

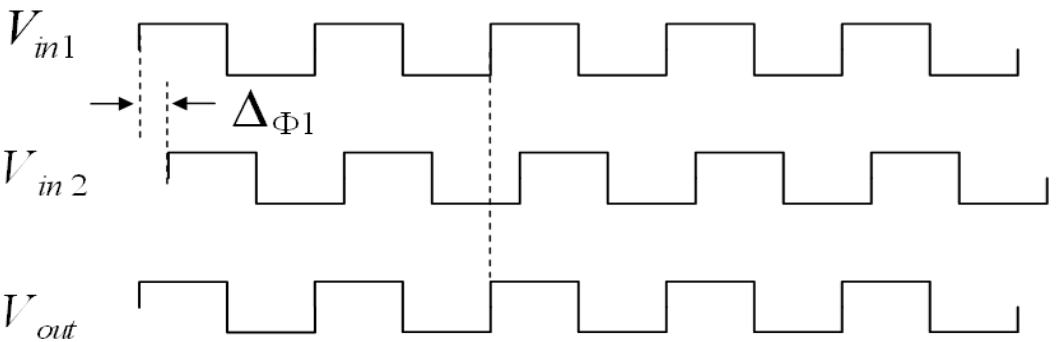


In the Locked Condition

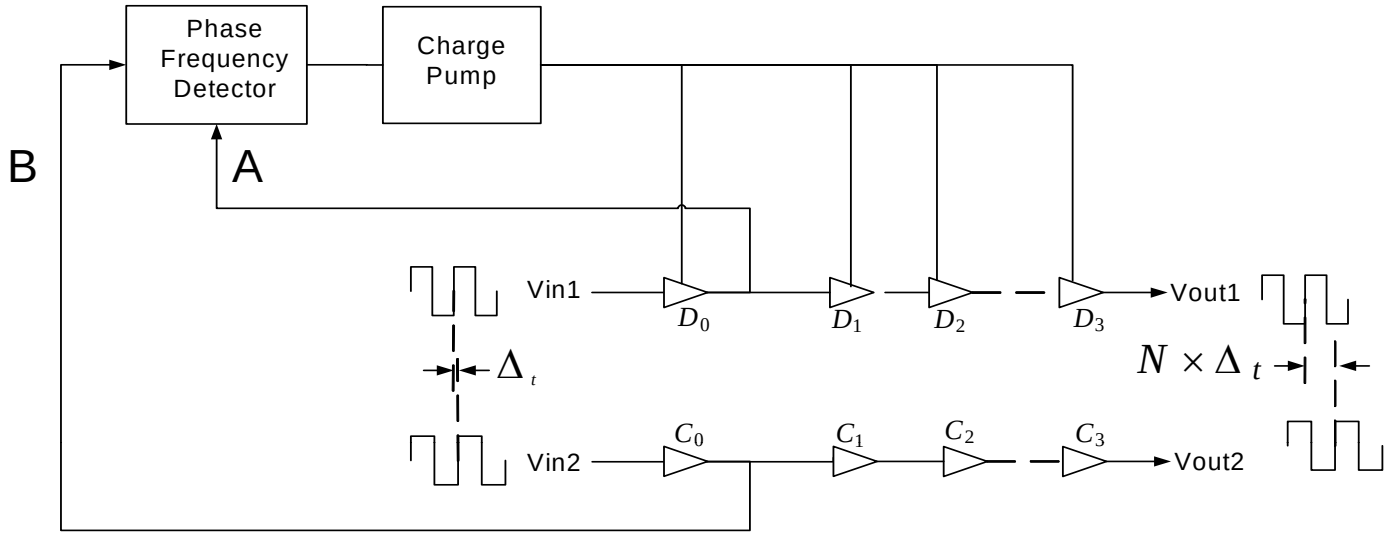
DLL Architecture with Two Distinct Inputs







Block Diagram of the Proposed Time Amplifier



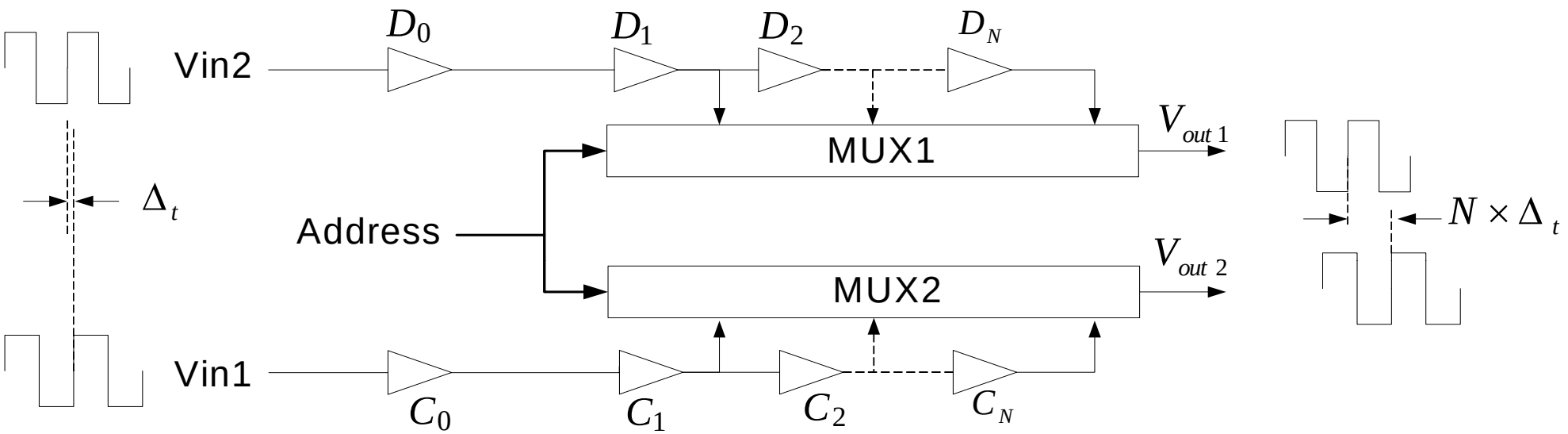
At the Locked state

$$\Phi_A = \Phi_B$$

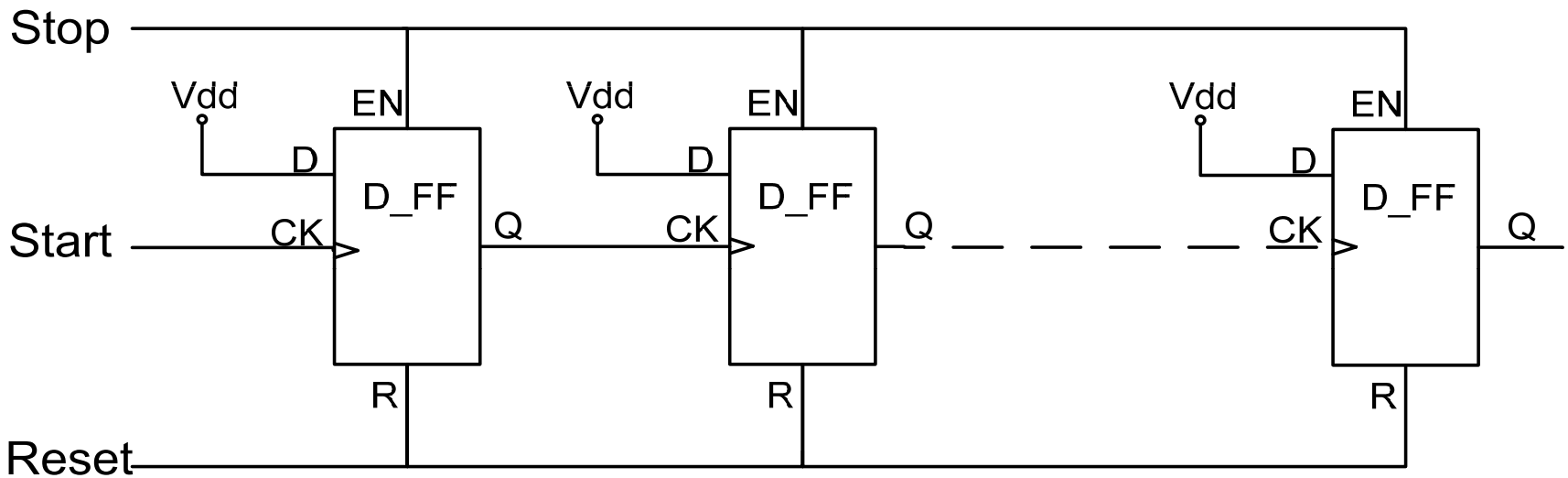
$$\Phi_{in1} + \frac{T_{D0}}{T} \times 2\pi = \Phi_{in2} + \frac{T_{C0}}{T} \times 2\pi$$

$$\Phi_{in1} - \Phi_{in2} = \frac{2\pi}{T} \times (T_{C0} - T_{D0})$$

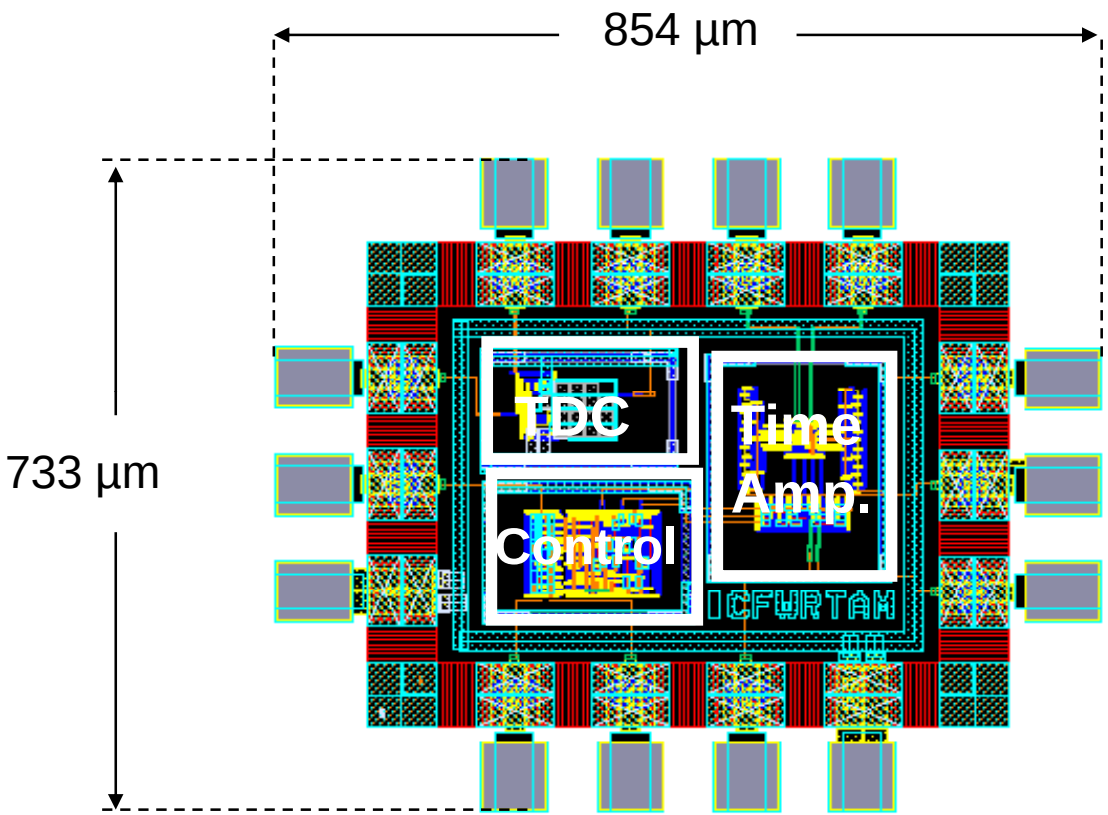
Two Delay Lines with Selectable Outputs



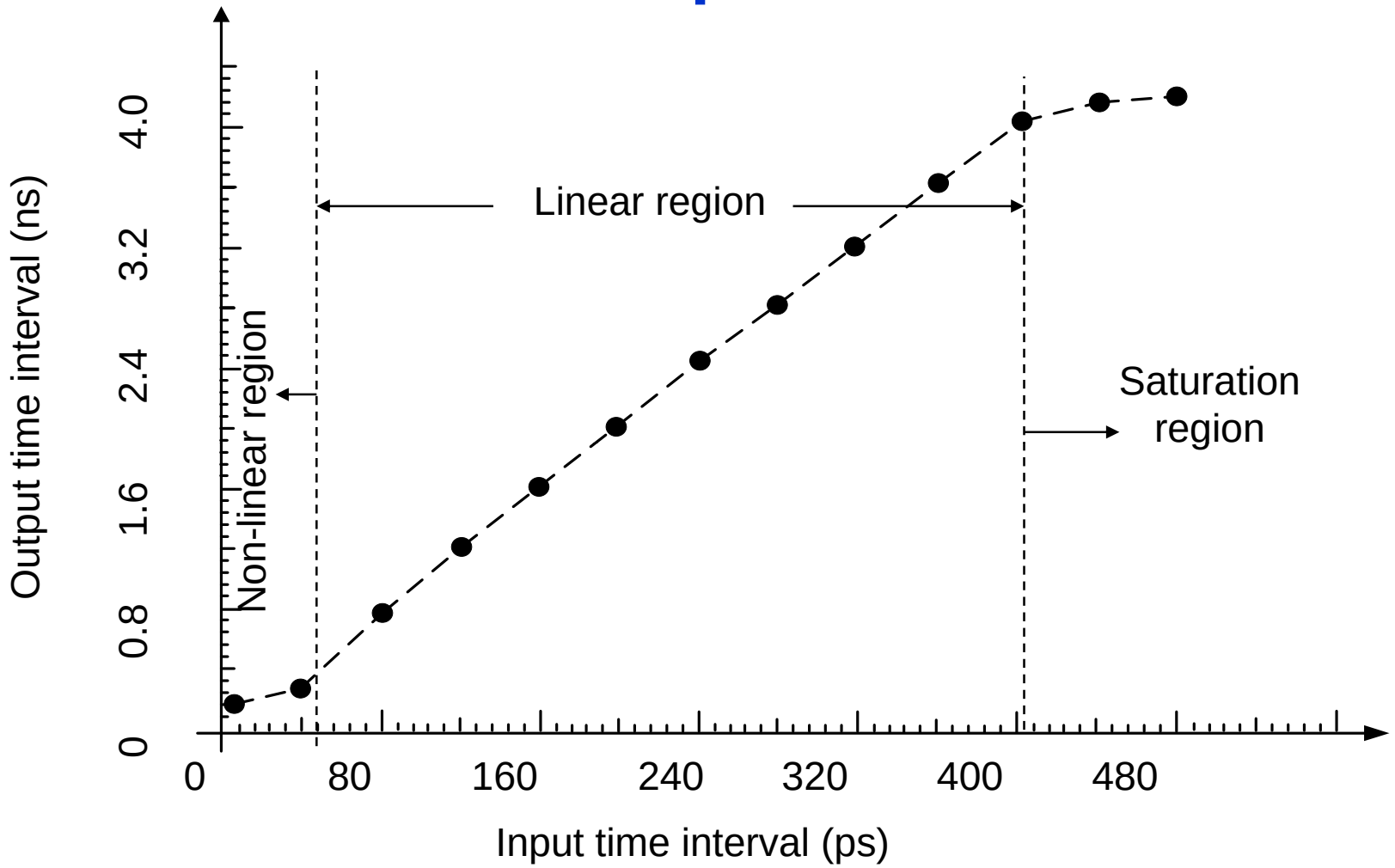
Schematic Diagram of the Employed TDC



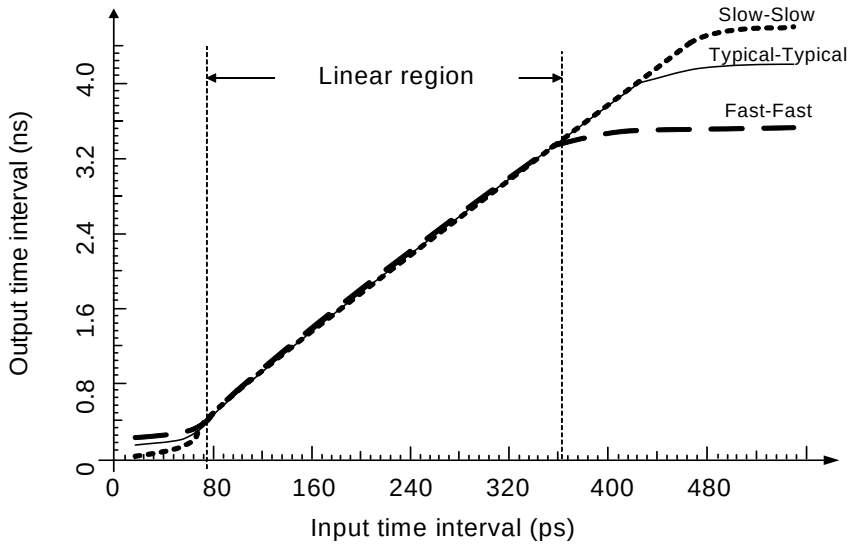
Layout of the Proposed Time Measurement System



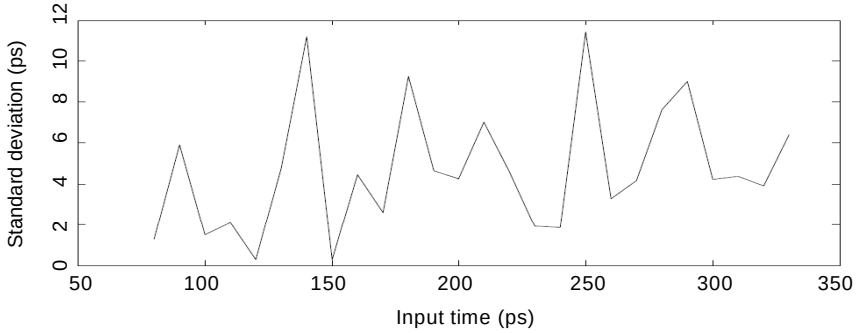
Transfer Characteristic of the Time Amplifier



Effect of process variations on Measurement Results



Input and output of the amplifier for fast-fast, slow-slow and typical-typical process corners



Standard deviation under the worst case process variations in the linear region.